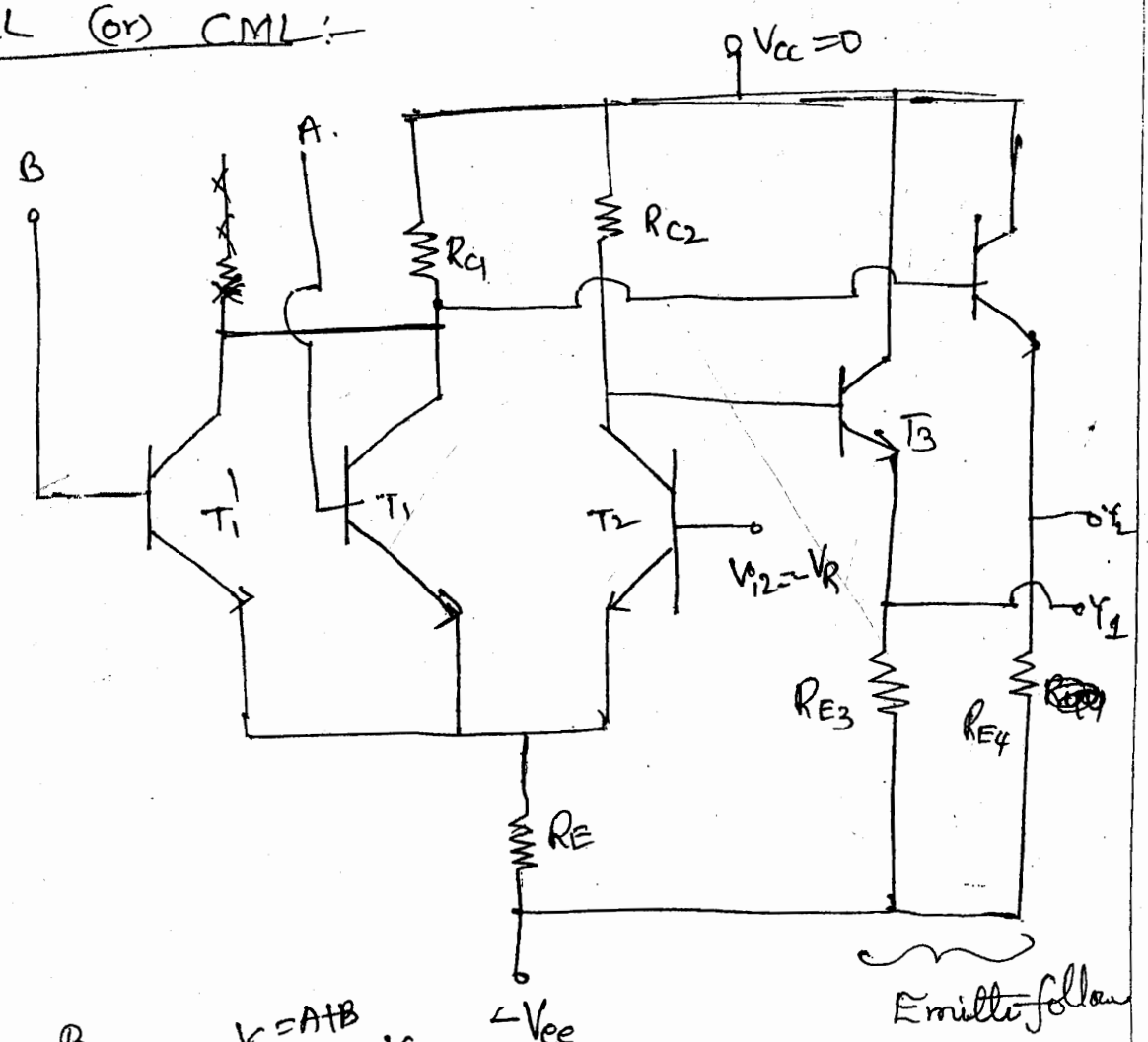
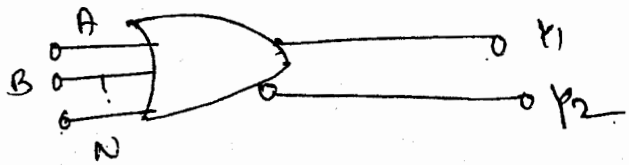
ECL (or) CML :-



A	B	$Y_1 = A+B$	$Y_2 = \overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0



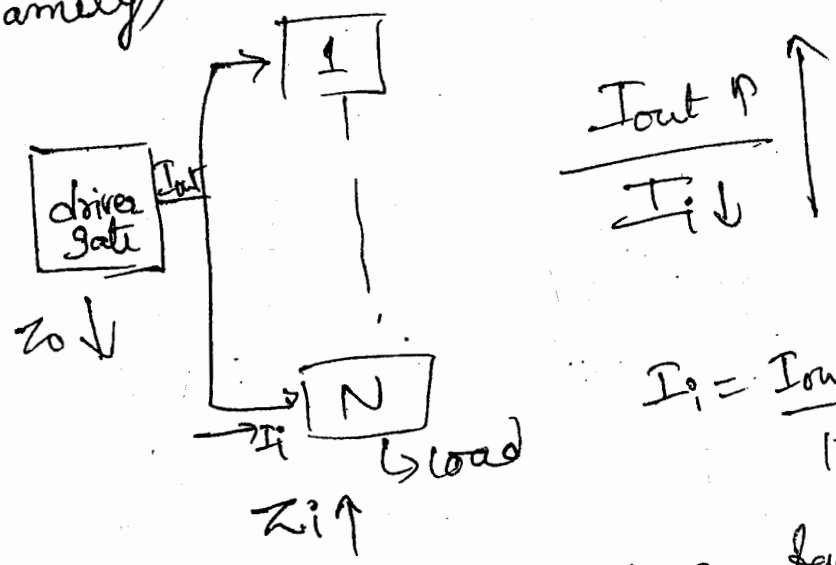
OR/NOR.

* Two Emitters are Connected at one point So it is called as Emitter Coupled Logic

Floating i/p in ECL can be treated as logic '0'

* Open Emitter Resistor in T_4. then it is called as ECL with open Emitter then this operation called as "Wired OR" operation *

* Fan-out of ECL is very large.
* The max no of logic gates which are possible to connect as a load to a driver gate is 'N' then the Fanout of driver gate is called 'N'. (The load & driver gate must belongs same logic family)



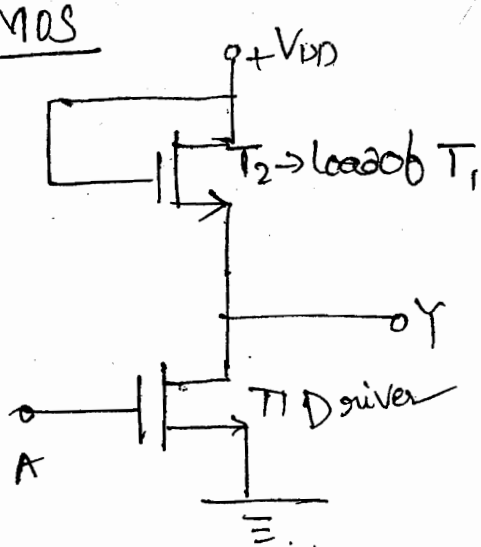
* Compared to DTL, TTL only ECL fan out is very high

fanout is high Bcz of high i/p impedance & low o/p impedance.

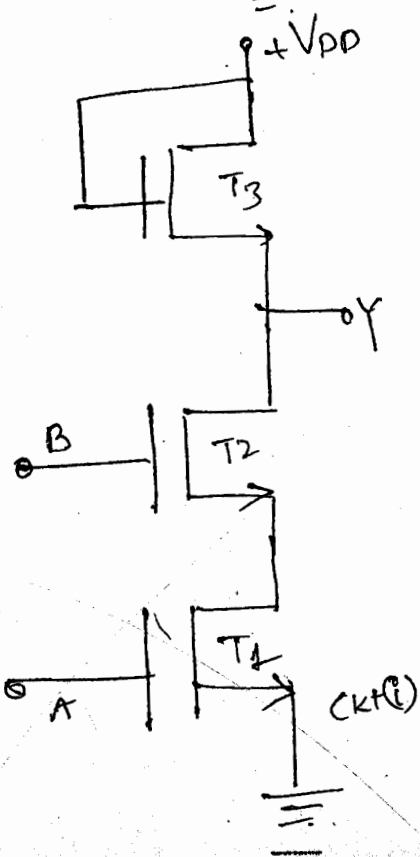
$P_D = V_{EE} \times I_{out}$

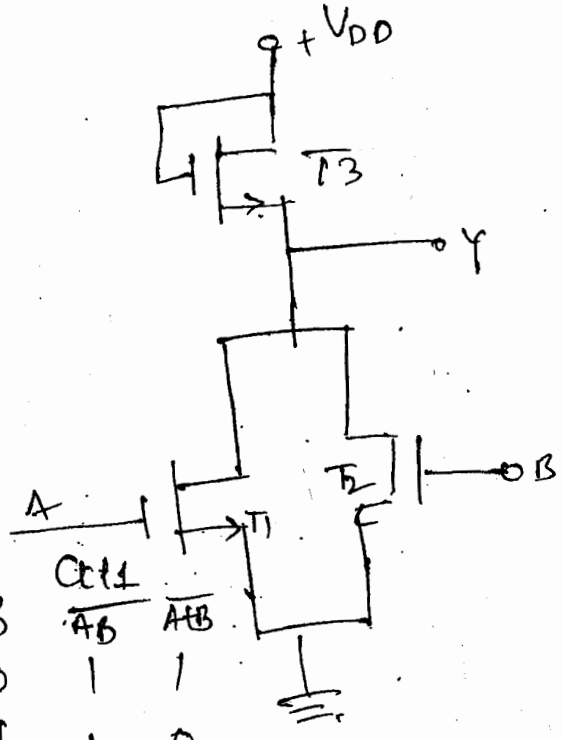
(Large amount of current drawn every time then power dissipation is very high. then propagation delay is very less.

NMOS



A	$Y = \bar{A}$
0	1
1	0

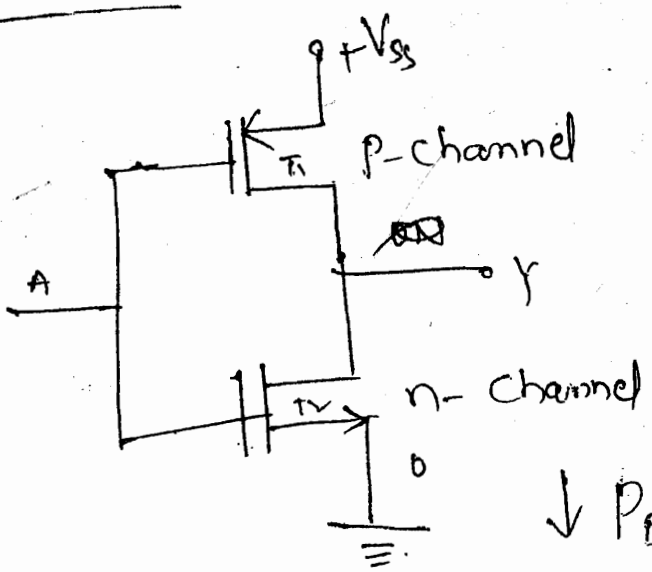




A	B	$\overline{AB}$	$\overline{A+B}$
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

* Power Consumption of NAND gate is Very less. Bcz By using only one i/p is '1', we can get all o/p's. where as in NOR gate is not like that.

CMOS Inverter



A	$\bar{A} = Y$
0	1
1	0

$\downarrow P_D = V_{ss} \cdot I_{out} \downarrow$